UNITED STATES PATENT APPLICATION FOR:

SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES

Inventor(s):

Biju CHANDRAN

Carlos A. GONZALEZ

Prepared by:

Antonelli, Terry, Stout & Kraus, LLP
1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Tel: 703/312-6600
Fax: 703/312-6666

SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES

Field

The invention relates to an improved low resistance package-to-die interconnect scheme for reduced die stresses, and particularly to an electronic assembly/semiconductor package employing the same. A method of interconnecting a die and substrate according to the invention is also disclosed.

Background

A conventional die to package interconnect architecture is illustrated in Figs. 1-3 of the drawings. In the prior art semiconductor package 1, the interconnect scheme between die 2 and substrate 3 comprises copper bumps 4 which are electroplated on the die, and eutectic AgSn solder 5 which is paste printed on the substrate lands. Soldered joints are formed in the conventional process by placing the die with copper bumps and the substrate with contact lands or pads to which solder has been applied in contact with one another and heating the die and substrate together to a temperature higher than the solder

melting temperature, followed by cooling the soldered assembly. The solder on the contact pads of the substrate is reflowed during this joining process to wet the copper standoffs on the die to form the soldered joints.

The die in the conventional package comprises thin film, inter layer dielectric (ILD) layers 6, see Fig. 4, on its front, lower surface under the copper bumps of the interconnect architecture. Due to the inherent weakness (cohesive and adhesive strengths) of the ILD material, stresses on the dielectric layers during reliability testing of the package can cause gross delamination of the ILD interfaces. A current focus for addressing the reliability issue posed by such ILD delamination in the die is on increasing the ILD material cohesive and adhesive strengths by modifying its chemistry, and by interface toughening schemes.

The ILD material that is typically used is carbon doped oxide. However, other ILD materials being evaluated for possible use are significantly weaker than the carbon doped oxide ILD material. Measurements on candidate materials indicate they are in some cases 10 to 100 times, e.g., at least about an order of magnitude, weaker than carbon doped oxide. These materials may be too weak to be accommodated in dies which are to be packaged using the current package-to-die interconnect architecture. An improved, low resistance package-to-die

interconnect scheme for reducing die stresses would make it possible to use these significantly weaker ILD materials in the packaged die.

Brief Description of the Drawings

Fig. 1 is a schematic illustration of a current interconnect scheme.

Fig. 2 is an enlarged view of a portion of the prior art interconnect scheme within the box A of Fig. 1.

Fig. 3 is a schematic view of the die with copper bumps of the conventional interconnect scheme of Figs. 1 and 2.

Fig. 4 is an enlarged view of a portion of the die with copper bumps within the circle B in Fig. 3, marked with the line b-b1 for stress plots, and showing thin film ILD layers in the lower, front surface of the die under a copper bump.

Fig. 5 is a schematic drawing of the die with ILD layer and copper bump wherein stresses in the ILD layer when the die is subjected to a thermal transient are shown in a stress contour plot along the ILD layer wherein the more darkly shaded region represents the region of highest stresses.

Fig. 6 shows plots of peeling stress in the ILD layer as a function of distance along the die bump for a copper bump of the prior art interconnect

scheme and for two solder die bumps according to the present invention, when heated to the same temperature.

Fig. 7 is a comparison of normalized ILD peeling stress for the interconnect scheme of the present invention wherein a copper bump is provided on the substrate and the prior art interconnect scheme of Figs. 1-3 where the copper bump is on the die.

Fig. 8 is a schematic illustration of an interconnect scheme/electronic assembly/semiconductor package of an example embodiment of the present invention.

Fig. 9 is an enlarged view of a portion of the interconnect scheme of Fig. 8 shown within the box C.

Fig. 10 is a schematic illustration of the die and substrate for making the interconnect scheme of Figs. 8 and 9, shown before contacting the solder bump on the die with the copper contact member/bump on the substrate for soldering.

Detailed Description

An example embodiment of a package 7 with a package-die interconnect scheme according to the present invention is depicted in Figures 8-10. The package utilizes copper bumps 8 on a substrate 9 and solder bumps 10 on a die

11. In the example embodiment, the lower yield strength solder material, a AgSn solder in the example, acts as the die bump. The solder is electroplated on the die to form the die bumps 10. The copper bumps 8 on the substrate may be copper columns or studs, as needed. They are electroplated on the substrate lands or pads to provide standoffs, and to lower the resistance of the interconnect. If copper columns are not needed for performance, a solder with a melting temperature higher than the melting temperature of the solder on the die could be electroplated on the substrate for stand-off.

The present invention addresses the problem of ILD delamination under the die bumps during temperature cycling of the package by lowering the yield strength of the die bump material in relation to the copper or other conductive material of the contact member/stand-off on the substrate. This change has been found to help ILD integrity. Lowering the yield strength of the die bump material reduces the stresses transferred to the die (simplistically, the bump deforms inelastically absorbing energy). More specifically, crystal structure correlations, and measurements indicate that the yield strength of the electroplated copper used for the die bumps in the conventional interconnect scheme of Figs. 1-3, is in the 350-450 MPa range, making the bump extremely stiff. During temperature excursions (before and after die-attach), this stiff bump induces a significant

amount of normal stresses on the dielectric layers in the die. These stresses cause gross delamination of the ILD interfaces during reliability testing. Modeling indicates that the biggest single contributor effecting ILD stresses on the die is the yield strength of the die bump. In many packages, performance requirements necessitate the use of electrically conductive standoffs/copper bumps in the interconnect stack-up. The present invention provides a method to incorporate the copper bumps in the interconnect stack-up, while significantly reducing the stresses in the ILD material.

Lowering the yield strength of the die bump material in accordance with the present invention has been shown by modeling to reduce the stresses transferred to the die. This benefit of the invention is also borne out by reliability test results comparing ILD cracking with Cu die bumps and high lead solder die bumps according to the invention. Putting the material that melts during chip-join on the die, enables the use of a modified "instant-chip-join" like die-attach process according to the invention to significantly reduce coefficient of thermal expansion mismatch induced stresses (and die warpage) from soldering. In this process, the die with solder die bumps is heated to a temperature above the melting temperature of the solder of the die bumps, apart from the substrate. The substrate is preferably heated only to a substantially lower temperature and the

two components are then joined for soldering the die to the substrate. The differential heating of the die and substrate exploits the principle that if elongation of the adherents, the die and substrate, at the temperature the solder solidifies, are the same, then, the coefficient of thermal expansion (CTE) mismatch induced stresses between the die and substrate from soldering can be minimized.

The modeling or simulation results comparing the interconnect scheme of the present invention with the conventional interconnect scheme of Figs. 1-3 are illustrated in the drawings. That is, Figs. 3 and 4 show details of a copper bump on the die of the conventional interconnect scheme of Figs. 1 and 2, and the thin film ILD region under the bump. During heating and cooling the bare die, the CTE mismatch between the materials in the die cause stresses and strains in the thin film ILD layers in the die as shown in Fig. 5. In Fig. 5, the ILD layer represents a stress contour plot showing that the region 12 of highest stresses is at the edge of the copper bump, when the die is subjected to a thermal transient. The area under consideration is represented by the line B-B1 on the ILD layer in Fig. 4.

Fig. 6 compares the modeled stresses in the ILD layer along the line B-B1 (marked in Fig. 4), for different die bump materials, when they are subjected to

the same ΔT. Since the bump materials are electroplated at room temperature, room temperature is the stress-free state for the die. Heating (and cooling) induces CTE mismatch stresses on the die thin film layers due to the bump, as shown in Fig. 6. The peeling stress at the edge of the bump is markedly lower with the lead tin and silver tin solder materials used in accordance with the present invention, as compared with the copper die bump of the conventional interconnect scheme.

Since ILD delamination is the key failure mode, only the normal component of stress (peeling stress) is being compared in Fig. 6. It should be noted that even though the compressive peeling stress at the die edge (produced during heating the bare die) is in itself not a big concern, cooling the die reverses the direction of the stresses. Also, interaction of the package induced stresses with this copper bump induced stresses during different thermal loading conditions creates a significant increase in ILD stresses with the copper bump.

Fig. 7 compares the maximum ILD peeling stress for two different die-bump/substrate bump/substrate combinations. For a case where the copper bump is on the substrate as in the present invention (the right side column in Fig. 7), as compared with the conventional interconnect scheme where the copper bump is on the die (the left side column in Fig. 7), it is noted that the maximum peeling

stress after die-attach in the case of having the copper bump on the substrate is about half that of the current case where the copper bump is on the die. This difference is due to the large yield strength of electroplated copper (400 MPa) as opposed to the much lower yield strength for the AgSn solder (around 40 MPa at room temperature). The lower yield strength of the solder die bump of the present invention will relieve some of the stress (by undergoing local plastic deformation), without transferring it to the die ILD layers. The difference will be even more in the case of temperature cycling, where the cooling cycle will make the residual stress at the bump edge (shown in Fig. 6) positive, increasing the stress for the case where the copper bump is on the die. To put the 50% reduction in ILD stresses with the AgSn/Cu/organic material substrate (OLGA) combination of the invention (in the right side of Fig. 7) in perspective, the reduction in ILD stresses by going to a ceramic substrate (Cu/AgSn/ceramic) with 6.5 ppm/°C CTE is only about 20%. Note, that even though the substrate in the conventional package of Figs. 1-3 and the substrate in the package of the present invention illustrated in Figs. 8-10 is a low cost organic substrate, this method can be applied to other common substrate materials like ceramic. However, the plastic and organic substrate materials have relatively high CTEs, along the order of 17 ppm/°C. The relatively larger CTE mismatch in packages

using the higher CTE package substrate materials, where the silicon semiconductor chip typically has a CTE of about 2.6-3.3 ppm/°C, can induce higher ILD stresses.

This concludes the description of the example embodiment. Although the present invention has been described with reference to one illustrative embodiment thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. For example, convention die attach reflow process was used to demonstrate the ILD stress reduction using this invention in the example embodiment. Even more stress reduction can be obtained by combining this invention with a modified die attach process which makes the thermal expansion of the chip and the substrate before soldering the same or substantially the same due to separate heating of each to a different temperature in relation to their CTEs. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts

and/or arrangements, alternative uses will also be apparent to those skilled in the art.